

# 8bit 3ch D/A converter

## BH2220FVM

BH2220FVM is 8bit 3 channel D/A converter for electronic adjustment. The 3-channel DC output can be independently controlled by three-wire serial interface from micro-controller.

The D/A converter can generate without loss by Rail to Rail output within the setting voltage.

This small MSOP8 package is suitable for portable appliances.

### ●Applications

The voltage adjustment for DVC, DSC etc.

### ●Features

- 1) 8bit 3-channel D/A converters adopting R-2R system.
- 2) 3-wire 10-bit serial interface.
- 3) POWER ON RESET circuit.
- 4) The full scale output voltage range : 2.7V~5.5V.
- 5) MSOP8 package.

### ●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>CC</sub>	-0.3~+7.0	V
Maximum output voltage	V <sub>IN</sub>	-0.3~V <sub>CC</sub>	V
Storage temperature	T <sub>stg</sub>	-55~+125	°C
Power dissipation	P <sub>d</sub>	310 *	mW

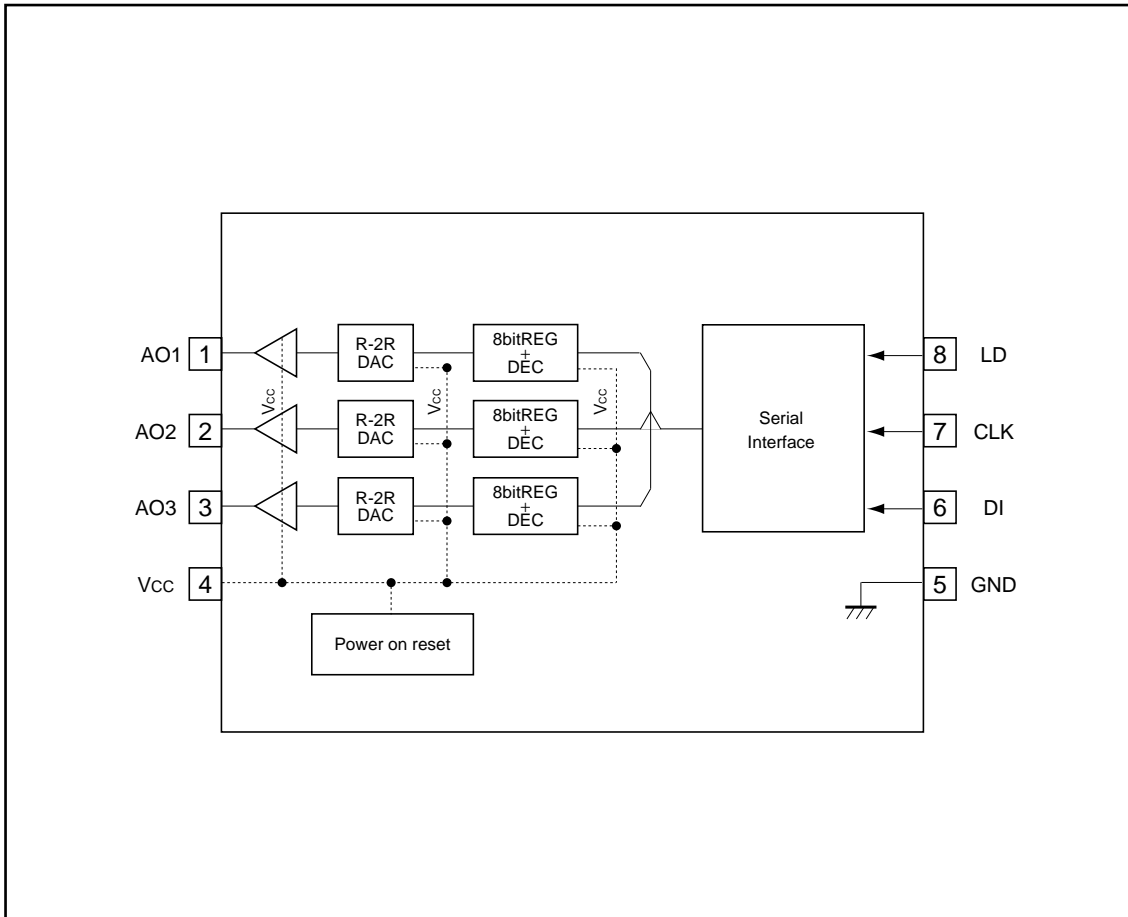
\*Reduced by 3.1mW for each increase in Ta of 1°C over 25°C.

©This product is not designed for protection against radioactive rays.

### ●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
V <sub>CC</sub> supply voltage	V <sub>CC</sub>	2.7	-	5.5	V
Analog output source current	I <sub>oL</sub>	-	-	1.0	mA
Analog output sink current	I <sub>oH</sub>	-	-	1.0	mA
Operating temperature range	T <sub>opr</sub>	-20	-	85	°C
Clock frequency	FSCLK	-	1.0	-	MHz
Limit load capacitance	CL	-	-	0.1	μF

●Block diagram



## Standard IC

## ●Pin descriptions

Pin No.	Symbol	In / Out	Description
1	AO1	OUT	Analog output pins
2	AO2	OUT	
3	AO3	OUT	
4	V <sub>CC</sub>	–	Power supply pin
5	GND	–	Common GND pin
6	DI	IN	Serial Data input pin
7	CLK	IN	Serial Clock input pin
8	LD	IN	Serial Load input pin

●Electrical characteristics (unless otherwise noted, T<sub>a</sub>=25°C, V<sub>CC</sub>=3.0V, R<sub>L</sub>=OPEN, C<sub>L</sub>=0pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<Operating current> (80H set)						
V <sub>CC</sub> system	I <sub>CC</sub>	–	0.4	0.8	mA	CLK=1MHz
<Logic interface>						
Input low voltage	V <sub>IL</sub>	GND	–	0.2V <sub>CC</sub>	V	
Input high voltage	V <sub>IH</sub>	0.8V <sub>CC</sub>	–	V <sub>CC</sub>	V	
Input low current	I <sub>IL</sub>	–	–	10	μA	
Input high current	I <sub>IH</sub>	–	–	10	μA	
<Buffer amplifier>						
Minimum output voltage	ZS1	GND	–	0.1	V	00H set I <sub>OH</sub> =0.0mA
	ZS2	GND	–	0.2	V	00H set I <sub>OH</sub> =0.5mA
	ZS3	GND	–	0.3	V	00H set I <sub>OH</sub> =1.0mA
Maximum output voltage	FS1	V <sub>CC</sub> – 0.1	–	V <sub>CC</sub>	V	FFH set I <sub>OL</sub> =0.0mA
	FS2	V <sub>CC</sub> – 0.2	–	V <sub>CC</sub>	V	FFH set I <sub>OL</sub> =0.5mA
	FS3	V <sub>CC</sub> – 0.3	–	V <sub>CC</sub>	V	FFH set I <sub>OL</sub> =1.0mA
<DAC accuracy>						
Resolution	RES	–	8	–	bit	
Differential nonlinearity error	DNL	–1.0	–	1.0	LSB	Input code 02H–FDH
Nonlinearity error	INL	–1.5	–	1.5	LSB	Input code 02H–FDH

Standard IC

●Circuit operation

(1) Power on reset

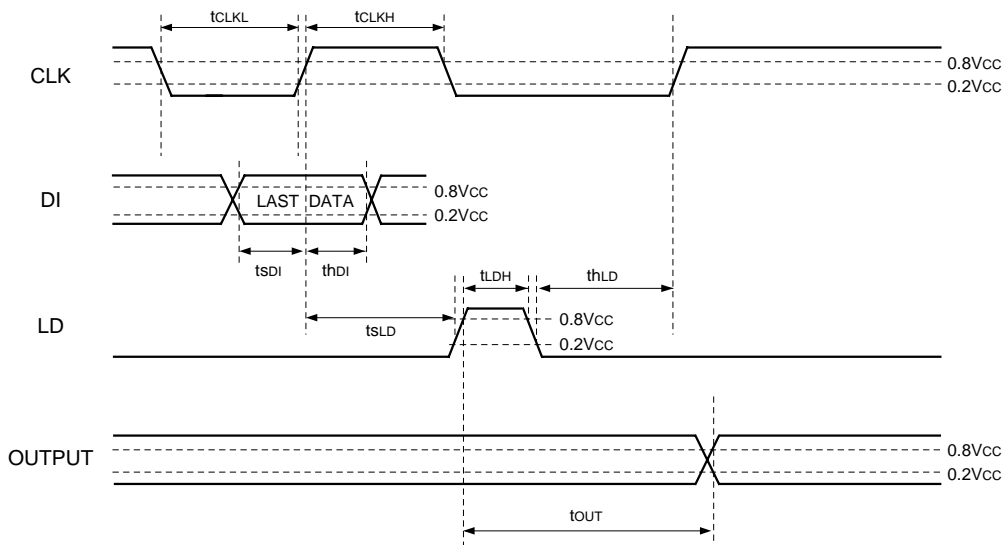
This LSI has a power on reset circuit that sets an analog output to low level in V<sub>CC</sub> power stand-up.

Please be sure that the time constant meets below condition, because the output is undefined when V<sub>CC</sub> power stand up too rapidly.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V <sub>CC</sub> supply voltage rise time	TrV <sub>CC</sub>	10	–	–	ms	V <sub>CC</sub> =0→2.7V
Power on reset voltage	VPOR	–	1.9	–	V	

(2) Conditions of operating timing (unless otherwise noted, Ta=25°C, V<sub>CC</sub>=3.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK L level pulse width	t <sub>CLKL</sub>	200	–	–	ns	
CLK H level pulse width	t <sub>CLKH</sub>	200	–	–	ns	
DI setup time	t <sub>SDI</sub>	30	–	–	ns	
DI hold time	t <sub>hDI</sub>	60	–	–	ns	
LD setup time	t <sub>SLD</sub>	200	–	–	ns	
LD hold time	t <sub>hLD</sub>	100	–	–	ns	
LD "H" level pulse width	t <sub>LDH</sub>	100	–	–	ns	
Analog output delay time	t <sub>OUT</sub>	–	–	300	μs	C <sub>L</sub> =50pF, R <sub>L</sub> =10kΩ
		–	–	100	μs	C <sub>L</sub> =50pF, R <sub>L</sub> =0.5MΩ



\*A signal level is judged at 80% or 20% of V<sub>CC</sub>

Standard IC

(3) Command sending

Control command is 3wire 10bit serial interface. (MSB first)

Data is taken in with the rise edge of the CLK and output data is fixed in the LD high section.

Data is maintained in the LD low section.

LSB (LAST)								MSB (FIRST)	
Data set								Channel select	
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9

•Data set

D0	D1	D2	D3	D4	D5	D6	D7	Analog output voltage level
0	0	0	0	0	0	0	0	GND
1	0	0	0	0	0	0	0	(Vcc-GND) / 256×1
0	1	0	0	0	0	0	0	(Vcc-GND) / 256×2
1	1	0	0	0	0	0	0	(Vcc-GND) / 256×3
0	0	1	0	0	0	0	0	(Vcc-GND) / 256×4
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	(Vcc-GND) / 256×254
1	1	1	1	1	1	1	1	(Vcc-GND) / 256×255

•Channel select

D8	D9	Adress select
0	0	AO1
1	0	AO2
0	1	AO3
1	1	Don't Care

●Operation notes

(1) Regarding to the DNL & INL

This item is guaranteed under below condition.

Input code 02H-FDH

(2) Regarding to the power on reset function

This function operates detecting the voltage level of the Vcc.

So, if the voltage level of the Vcc become less than power on reset voltage when working, it is a possibility that the outputs become reset condition.

●External dimensions (Units : mm)

